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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/005,513	11/08/2001	James Joseph Brogle	TYCO-017XX	9175

207 7590 04/01/2003

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EXAMINER	
FOONG, SUK SAN	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,513	BROGLE ET AL.	
	Examiner	Art Unit	
	Suk-San Foong	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 4 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The structure recited in claim 4, lines 2-4, is recited in claim 1, lines 16-20.

2. Claim 7 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The structure recited in claim 7, lines 2-4, is recited in claim 1, lines 4-6.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 5, 6 and 11-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The term "low-loss" in claim 3, line 3 is a relative term which renders the claim indefinite. The term "low-loss" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

6. Claim 5, line 3, it is not clear what is recited through the term “thin”.

7. Claims 11 and 12, recites the limitation "the first forming step" in line 1. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 13, recites the limitation "the second forming step" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

9. Claims 14-16, recites the limitation "the third forming step" in line 1, lines 1-2 and lines 1-2, respectively. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 15, line 2, it is not clear what is recited through the term “thin”.

11. Claim 16, line 3, the use of "predetermined" reads on a nebulous mental step conducted prior to the manipulative steps of the claimed invention, hence rendering the present process claims unclear in meaning and scope. If applicant wishes to patent detailed controls over the recited process, they must be positively recited.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Calligaro ('822).

Calligaro discloses a microwave integrated circuit device which includes semiconductor substrate 3 such as silicon and GaAs (Col. 1, lines 18-23, Col. 2, lines 40-42, and Fig. 1), at least one first mesa portion 5 and at least second mesa portion 4 on substrate 3 (Col. 2, lines 46-47), at least one PIN diode formed on first mesa portion 5 and including a PIN anode region (Col. 3, lines 25-27), at least one Schottky diode formed on second mesa portion 4 and including a Schottky anode region (Fig. 1), passivation layer 10 comprised of glass material (Col. 2, lines 62-68) deposited over first and second mesas 5 and 4 while providing access to at least the PIN anode region and the Schottky anode region (Col. 2, lines 54-58) and wherein the PIN anode region 9 and Schottky anode region 7 are formed in plane 3 (Col. 3, lines 10-18).

14. Claims 8-10 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Calligaro ('822).

Calligaro discloses forming a microwave integrated circuit device which includes providng semiconductor substrate 2 such as silicon and GaAs and epitaxial layers (Col. 1, lines 18-23, Col. 2, lines 40-42, Col. 3, lines 31-34 and Fig. 1), forming at least one first mesa portion

5 and at least second mesa portion 4 on substrate 3 (Col. 2, lines 46-47) by a single etching operation (Col. 4, lines 10-15), then forming at least one PIN diode on first mesa portion 5 and including a PIN anode region (Col. 3, lines 25-27), forming at least one Schottky diode on second mesa portion 4 and including a Schottky anode region (Fig. 1), then depositing passivation layer 10 comprised of glass material (Col. 2, lines 62-68) deposited over first and second mesas 5 and 4 while providing access to at least the PIN anode region and the Schottky anode region (Col. 2, lines 54-58) and wherein the PIN anode region 9 and Schottky anode region 7 are formed in plane 3 (Col. 3, lines 10-18).

Claim Rejections - 35 USC § 103

15. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calligaro ('822) as applied to claims 1-4 above, and further in view of Portnoy et al. (991) and Meyerson ('452).

Calligaro does not disclose that a thin epitaxial layer of the Schottky anode is in the Schottky diode region of the substrate.

Portnoy et al. teaches a structure of a Schottky diode in semiconductor devices which includes semiconductor substrate 16 (Col. 4, lines 65-67 and Fig. 1), epitaxial layer 14 formed on exposed surface of substrate 16 (Col. 5, lines 49-53), passivation layer 22 formed over substrate 26 (Col. 5, line 66 to Col. 6, lines 5), and Schottky anode 12 (Col. 6, lines 22-26).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Portnoy et al. with Calligaro because it would enable the epitaxial layer of Portnoy et al. formed in the Schottky anode region of the combination and, furthermore, choose the

concentration of the epitaxial layers of the combination according to the teachings of Portnoy et al. and obtain further advantage of making the areal junction capacity very low and extending the depletion region all the way to the surface of the low resistivity substrate thereby leaving no undepleted epitaxial material (Portnoy et al., Col. 4, lines 41-50).

The combination does not teach that the thin epitaxial layer is formed by ultra-high vacuum chemical vapor deposition process.

Meyerson teaches that thin epitaxial layers are formed semiconductor substrates by ultra-high vacuum chemical vapor deposition process (Col. 7, line 24 to Col. 8, line 23).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Meyerson with the combination because it would enable the structure of the thin epitaxial formed in the Schottky anode region of the combination and obtain further advantage of eliminating the problems of autodoping and solid state diffusion (Meyerson, Col. 5, lines 35-36).

The choice of thickness of the thin epitaxial layer would have been a matter of routine optimization to achieve the desired device density and the desired device characteristics of the device to be formed. (See MPEP 2144.05).

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Calligaro ('822) as applied to claims 1-4 above, and further in view of Goodrich et al. ('310).

Calligaro does not teach that the first and second mesa portions are formed by a single anisotropic etching operation.

Goodrich et al. discloses a monolithic microwave circuits which includes semiconductor substrate 26 comprised of silicon material (Col. 4, lines 11-22, Col. 5, lines 1-5, and Fig. 5), PIN

diode 10 in a PIN diode region of substrate 26 and other features/components 71, 73 in second regions of substrate 26 (Col. 7, lines 13-19, 33-36, and Fig. 17C) formed on first and second mesa portions on substrate 26 by perfoming a single etching process using an anisotropic etching or wet chemical etching method (Col. 6, line 65 to Col. 6, line 7, and Figs. 11, 14 and 17A).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Calligaro with Goodrich et al. because it would obtain the structure of the first and second mesas of Calligaro.

17. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calligaro ('822) as applied to claims 8-10 and 14 above, and further in view of Goodrich et al. ('310).

Calligaro does not teach forming first and second mesa portions by a single anisotropic etching operation.

Calligaro does not teach the step as recited in claim 12, lines 1-10.

Calligaro does not teach forming a PIN diode comprising the step as recited in claim 13, lines 1-7.

Goodrich et al. teaches a method of forming monolithic microwave circuits which includes providing semiconductor substrate 26 comprised of silicon material (Col. 4, lines 11-22, Col. 5, lines 1-5, and Fig. 5), then forming PIN diode 10 in a PIN diode region of substrate 26 and other features/components 71, 73 in second regions of substrate 26 (Col. 7, lines 13-19, 33-36, and Fig. 17C) by etching insulating layer 14 to form implant window 15 while remaining insulating layers 14a and 14b are masking other non-PIN diode regions of substrate 26 (Col. 5, lines 6-8, lines 13-16, and Fig. 7) and then implanting a dopant through implant window 15 to

form PIN anode 24 in the PIN diode region of substrate 26 while masking the other regions of substrate 26 covered by insulating layers 14a and 14b (Col. 5, lines 24-26, and Fig. 8), then depositing silicon nitride layer 28 the PIN diode region and other non-PIN diode regions of substrate 26 (Col. 5, lines 38-43, and Fig. 9), subsequently masking PIN diode region and other features/components 71, 73 in second regions of substrate 26 (Col. 5, lines 16-23 and 62-64), then etching portions of silicon nitride layer 28 except in the masked PIN diode region and other non-PIN diode regions of substrate 26 (Col. 5, lines 51-55, and Fig. 10), then performing a single etching process using anisotropic etching or wet chemical etching method to form first and second mesa portions on substrate 26 (Col. 6, line 65 to Col. 6, line 7, and Figs. 11, 14 and 17A), subsequently depositing passivation layer 62 such as glass on substrate 26 (Col. 7, lines 31-37 and Fig. 17B), and then forming PIN anode in the PIN diode regions and other metallization or contact for other features/components 71, 73 in second regions of substrate 26 (Col. 8, lines 2-11, and Fig. 17C).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Calligaro with Goodrich et al. because it would enable formation of the PIN diode of Calligaro to be performed and obtain further advantage of maintaining high quantity of stored charge while exhibiting minimal capacitance as opposed to the conventional mesa-type PIN diode as shown in Fig. 1 which decreases the amount of charge which may be stored (Goodrich et al., Col. 2, lines 33-37).

18. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calligaro ('822) as applied to claims 8-10 and 14 above and further in view of Goodrich et al.

('310) as applied to claims 11-13 above, and further in view of Portnoy et al. (991) and Meyerson ('452).

The combination process does not teach forming a thin epitaxial layer of the Schottky anode in the Schottky diode region of the substrate while masking the PIN diode region of the substrate.

Portnoy et al. teaches a method of forming a Schottky diode in semiconductor devices which includes providing semiconductor substrate 16 (Col. 4, lines 65-67 and Fig. 1), then forming and patterning masking layer 20 to expose a portion of substrate 16 where epitaxial layer 14 is to be formed with the disadvantage that spurious growth of the epitaxial material occurs (Col. 1, lines 30-34, Col. 5, lines 19-47, and Fig. 2), then forming epitaxial layer 14 on exposed surface of substrate 16 (Col. 5, lines 49-53), subsequently depositing passivation layer 22 over substrate 26 (Col. 5, line 66 to Col. 6, lines 5), and then forming Schottky anode 12 (Col. 6, lines 22-26).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Portnoy et al. with the combination process because it would enable formation of epitaxial layer of Portnoy et al. in the Schottky anode region of the combination process and thus choose the concentration of the epitaxial layers of the combination according to the teachings of Portnoy et al. and obtain further advantage of making the areal junction capacity very low and extending the depletion region all the way to the surface of the low resistivity substrate thereby leaving no undepleted epitaxial material (Portnoy et al., Col. 4, lines 41-50).

The combination process does not teach forming the thin epitaxial layer by ultra-high vacuum chemical vapor deposition process.

Meyerson teaches a method of forming thin epitaxial layers on semiconductor substrates by ultra-high vacuum chemical vapor deposition process (Col. 7, line 24 to Col. 8, line 23).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Meyerson with the combination process because it would enable formation of the thin epitaxial in the Schottky anode region of the combination process to be performed and obtain further advantage of eliminating the problems of autodoping and solid state diffusion (Meyerson, Col. 5, lines 35-36).

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

March 20, 2003

George Fourson
Primary Examiner
Art Unit 2823